Garima Ghai

Dean (Academics)
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Education

- **Ph.D. in Computer Science & Engineering** — Graduation: **December 2010**
  University of North Texas, USA — GPA: **4/4**
- **M.S. in Computer Science & Engineering** — Graduation: **August 2006**
  University of North Texas, USA — GPA: **3.6/4**
- **B.E. in Computer Science & Engineering** — Graduation: **July 2004**
  Rajiv Gandhi Technical University, India — GPA: **8.5/10**
- **Higher Secondary** — Graduation: **Jan 2000**
  St. Theresa's Higher Secondary School, India — GPA: **8.5/10**
- **Senior Secondary** — Graduation: **Dec 1999**
  St. Joseph's Convent School, India — GPA: **7.5/10**

Professional Experience

Oriental University — May 12'- Present

Job Title: Dean (Academics)
Opp. Revati Range, Sanwer Road,
Indore (M.P.) 453555

Responsibilities:

- Handling publication of University magazine and University newsletter bi monthly.
- Prepare University level academic calendar.
- Planning and expanding current and new academic programs.
- Currently working for International / National Collaborations in the field of academics with University.
- Supervise declaration of results and award medals and degrees.
- Currently establishing more Centers of Excellence
- Promoting and serving as a model for faculty development programs and student development programs.

- Serving as a liaison with professional associations of the University and state/national regulatory accrediting agencies.
- Formed the syllabus and time table for entire Btech course.
- Assisted the Training & Placement Department with their placement procedure for BE, MBA and Pharmacy students.
- Coordinator of MTech program for CSE and EC department.

Aperia Solutions, Texas, USA April'11-Aug'11

Job Title: Business Analyst

14881 Quorum Drive, Suite 600
Dallas, TX 75254, United States

Responsibilities:

- Aperia expanded to become the preeminent provider of ETL, BI, and hosted solutions in a variety of industries. Aperia platforms scale with industry, processing massive volumes on time. The Software as a Service (SaaS) platforms support millions of end users creating billions of transactions per day, all with the speed and reliability required for business.
- Ensured that all the artifacts are in compliance with corporate SDLC policies and guidelines.
- Prepared BRD and converted into functional specifications using requirement management tool using Requisite Pro.
- Created UML diagrams such as use case diagrams, activity diagrams, and sequence diagrams using MS Visio.
- Designed Data Flow Diagrams (DFD's), Entity Relationship Diagrams (ERD's), and web page mock ups using modeling tools.
- Developed and maintain project plan using MS Project. Made sure that all the deliverables met its deadline.
- Facilitated JAD sessions with individual, group of clients and technical units.
- Performed Object Oriented Analysis (**OOA**) design and developed work flow diagrams using MS Visio.
- Created Risk Analysis documents and Risk Management Plan.
- Conducted functional walk-throughs and supervising the development of user manuals for customers.
- Provided staff training on products and applications.
- Maintained documents for change request and implemented procedures for testing changes. Ensured that changes met its end result.
- Provide technical and procedural support for User Acceptance Testing (UAT).

University of North Texas, Texas, USA Jan '09-Dec'10

Job Title: Research Analyst

1155 Union Circle
Denton, TX 76203, United States

Responsibilities:

- P3 (power-performance-process) aware optimization of a 90nm low power, high static noise margin SRAM (Static Random Access Memory).
- Design, layout and process variation analysis of a 7, 9 and 10 SRAM.
- Design, power and read SNM optimization of a single-ended 7T SRAM cell using Design of Experiments/ Integer Linear Programming approach.

- Design, power and performance optimization of a Nano CMOS SRAM using hybrid Design of Experiments/ Monte Carlo approach.
- Implemented Regression techniques for optimization of LC VCO/SRAM circuit.

Oriental Institute of Science & Technology, India Oct '06-Dec'09

Job Title: Dean Academics

Thakral Nagar, Raisen Road,
Bhopal- 462021, India.

Responsibilities:

- Developed OGI (Oriental Group of Institutes) website and updated the same time.
- Monitored student attendance, semester exams, syllabus and time table.

Sabre Holdings, Texas, USA Jan '06-Aug'06

Job Title: Business Analyst

3150 Sabre Drive
Southlake, Texas 76092

Responsibilities:

- Conducted user interviews, gathered requirements, analyzed the requirements using RUP methodology and documented the requirements using Rational Requisite Pro.
- Gathered requirements, organized team meetings requirements from business users, generated process models, & use-case models, and created business requirements document (BRD) & functional requirements document **(FRD).**
- Involved in Data Modeling of both Logical Design and Physical design of data warehouse and data marts in Star Schema and Snow Flake Schema methodology.
- Utilized the business and financial requirements to develop detailed user interface for the applicationprototype.
- Developed, designed and executed test cases for systems testing and User Interface Acceptance testing.
- Conducted joint requirements planning (JRP) sessions as a facilitator to gather requirements from the business area and to discuss different critical success factors of the project like **Operational Feasibility Analysis, Technical Feasibility Analysis, Cost Benefit Analysis & etc.**
- Use Cases and other Process Flow Models were designed using Visio and Rational Rose.
- Worked with developers and designers of Business process management (BPM) system to make sure development understands business process and detailed technical requirements.
- Developed and managed project plans, schedules, issues log created and business-technical conflicts.
- Responsible writing Test Plans, Test Cases and Test Scripts using manual and automated testing tools from Rational such as **Winrunner.**

University of North Texas, Texas, USA Aug '04-Jan'06

Job Title: Teaching Assistant

1155 Union Circle
Denton, TX 76203, United States

Responsibilities:

- Teaching Assistant for courses like Database Design, Software Development, Software Engineering, Robotics.
- Monitored a class of 55 MS students.
- For Software development, helped students in project development and project deliverables include code, documentation and presentation slides.
- In Software Engineering taught Load Runner and developed a project.
- Worked with load runner
- Recording Vuser script with Vugen
- The load test planning, load runner controller
- Enhancing vuser script
- Creating a ScenarioCreating a script list, creating the vuser list
- Running a scenario, configuring a scenario, running a scenario and reporting and tracking defects.
- Understand user requirements/views
- Analyze existing and future data processing needs
- Develop an enterprise data model that reflects the organization's fundamental business rules
- Develop and refine the conceptual data model, including all entities, relationships, attributes, and business rules
- Integrate and merge database views into conceptual model
- Apply normalization techniques
- Identify data integrity and security requirements
- Derive a physical design from the logical design taking into account application, hardware,
- Operating system, and data communications network requirements
- Utilize prototyping as a rapid application development (RAD) method to implement a PC database (e.g., Microsoft Access® for the PC).

Professional Activities

- Member, IEEE
- Member, IETE India.
- Participated in Microsoft Women in IT SUMMIT (December 18th-19th 2014)

- Authored/co-authored numerous peer-reviewed journal articles and (blind) reviewed conference publications in the disciplines of Computer Science and Electronics Engineering.
- The research articles have appeared in journals like Elsevier Microelectronics Journal and
- Journal of Low-Power Electronics.
- Conference papers have been presented at various ACM/IEEE sponsored conferences such as ACM Great Lakes Symposium on VLSI and International Conference on VLSI Design.
- Microsoft Technology Associate Certification in .NET Fundamentals (C#) and Database Fundamentals.

Publications

1. G. Thakral, S. P. Mohanty, D. K. Pradhan, and E. Kougianos, "DOE-ILP Based Simultaneous power and Read Stability Optimization in Nano-CMOS SRAM", Special Issue on VLSI Design 2010, ASP Journal of Low Power Electronics (JOLPE), Vol. 6, No. 3, October 2010.

2. G. Thakral, S. P. Mohanty, D. Ghai, and D. K. Pradhan, " A Combined DOE-ILP Based Power and Read Stability Optimization in Nano-CMOS SRAM", in Proceedings of the 23rd IEEE International Conference on VLSI Design (VLSID), pp. 45-50.

3. G. Thakral, S. P. Mohanty, D. Ghai, and D. K. Pradhan, "A DOE-ILP Assisted Conjugate-Gradient Approach for Power and Stability Optimization in High-κ/Metal-Gate SRAM", inProceedings of the 20th ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), pp. 323-328, 2010.

4. G. Thakral, S. P. Mohanty, D. Ghai, and D. K.Pradhan, "P3(Power-Performance-Process) Optimization of Nano-CMOS SRAM using Statistical DOE-ILP", in Proceedings of the 11th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 176-183, 2010.

5. R. R. Bani, S. P. Mohanty, E. Kougianos, and G. Thakral, " Design of a Reconfigurable Embedded Data Cache", in Proceedings of the 1st IEEE International Symposium on Electronic System Design (ISED), pp. 163--168, 2010.
6. D. Ghai, S. P. Mohanty, and G. Thakral, " Fast Optimization of Nano-CMOS Voltage-Controlled Oscillator using Polynomial Regression and Genetic Algorithm", Elsevier Microelectronics Journal (MEJ), Volume 44, Issue 8, August 2013, pp. 631--641.
7. D. Ghai, S. P. Mohanty, and G. Thakral, " Fast Analog Design Optimization using Regression based Modeling and Genetic Algorithm: A Nano-CMOS VCO Case Study", in Proceedings of the 14th IEEE International Symposium on Quality Electronic Design (ISQED), 2013, pp. 422--427.
8. D. Ghai, **S. P. Mohanty**, and G. Thakral, " Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 809--812.
9. D. Ghai, **S. P. Mohanty**, and G. Thakral, " Double Gate FinFET based Mixed-Signal Design: A VCO Case Study", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 177--180.
10. D. Ghai, **S. P. Mohanty**, G. Thakral, and O. Okobiah, " Variability- Aware DG FinFET-based Current Mirrors", in *Proceedings of the 23rd ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, 2014, pp. 347—352.
11. V. P. Yanambaka, S. P. Mohanty, E. Kougianos, D. Ghai, and G. Ghai, "**Process Variation Analysis and Optimization of a FinFET based VCO**", *IEEE Transactions on Semiconductor Manufacturing (TSM), Volume 30, Issue 02,* May 2017, pp. 126-134.